LISTING OF THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently amended) A process for forming a housing for electronic modules, comprising the steps of:

providing a substrate having one or more regions, the one or more regions comprising at least one semiconductor structure, the substrate having at least a first substrate side to be encapsulated and an underside, wherein the at least one semiconductor structure is located on the first substrate side;

providing a vapor-deposition glass source and a plasma source in one arrangement;

arranging the first substrate side in such a manner with respect to the vapor-deposition glass source that the first substrate side can be vapor-coated;

vapor-coating the first substrate side with a glass layer;

wherein the step of vapor-coating comprises the steps of:

generating vapor by generating an electron beam and impinging the electron beam onto a glass target of the vapor-deposition glass source,

producing an ion beam by ionizing a gas in a plasma generated by [[a]] the plasma source, and

directing the ion beam onto the substrate during the vapor-coating so as to additionally densify the glass layer ~~so that the glass layer has a helium leak rate of less than 10^{-7} mbar l s^{-1}~~.

2. (Cancelled).

3. (Previously presented) The process as claimed in claim 1, further comprising providing the substrate with a passivation layer on a second side that is on the opposite side from the first substrate side.

4. (Previously presented) The process as claimed in claim 1, wherein the substrate comprises a wafer, the process further comprising packaging of components which still form part of the wafer.

5. (Previously presented) The process as claimed in claim 1, further comprising vapor-coating a second substrate side with a glass layer.

6. (Previously presented) The process as claimed in claim 1, wherein the vapor-deposition glass source generates at least a binary glass system.

7. (Previously presented) The process as claimed claim 1, wherein the first substrate side is vapor-coated until the glass layer has a thickness in the range from 0.01 to 1000 μm on the first substrate side.

8. (Previously presented) The process as claimed in claim 1, wherein the step of providing the vapor-deposition glass source comprises providing a reservoir having organic constituents, and converting the organic constituents into the vapor state through application of a vacuum or through heating so that during the vapor-coating mixed layers comprising inorganic and organic constituents can be formed on the first substrate side.

9. (Previously presented) The process as claimed in claim 1, wherein the glass layer has a thickness in the range between 0.1 and 50 μm.

10. (Previously presented) The process as claimed claim 1, wherein the glass layer has a thickness in the range between 50 and 200 μm.

11. (Cancelled).

12. (Previously presented) The process as claimed in claim 1, wherein the glass target is a borosilicate glass comprising aluminum oxide and alkali metal oxide fractions.

13. (Previously presented) The process as claimed in claim 1, wherein the glass layer has a coefficient of thermal expansion that is virtually equal to that of the substrate.

14. (Previously presented) The process as claimed in claim 1, wherein the glass layer provides a hermetic seal.

15. (Previously presented) The process as claimed in claim 1, further comprising vapor deposting a plurality of glass layers onto the substrate.

16. (Previously presented) The process as claimed in claim 1, further comprising removing material from a second substrate side, the second substrate side being on the opposite side from the first substrate side.

17. (Previously presented) The process as claimed in claim 1, wherein the substrate includes a wafer having a plurality of the structures wherein the process further comprises dividing the wafer to form a plurality of electronic modules which each have first encapsulated sides.

18. (Cancelled).

19. (Previously presented) The process as claimed in claim 39, further comprising vapor coating the underside with the glass layer after the plastic layers have been removed from the underside and dividing up the wafer so that the plurality of electronic modules are encapsulated on both sides.

20. (Previously presented) The process as claimed in claim 19, wherein the glass layer on the underside has a thickness in the range from 1 to 50 μm.

21-33. (Cancelled).

34. (Previously presented) The process as claimed in claim 1, further comprising applying a layer of plastic above the glass layer.

35-38. (Cancelled).

39. (Previously presented) The process as claimed in claim 17, further comprising lithographing plastic layers on the substrate and removing the plastic layers from the underside.

40. (Cancelled).

41. (Previously presented) The process according to claim 1, wherein the semiconductor structure comprises an integrated circuit.

42. (Cancelled).

43. (New) The process as claimed in claim 1, wherein the glass layer has a composition, in percent by weight, comprising:

SiO_2 75 to 85;

B_2O_3 10 to 15;

Na_2O 1 to 5;

Li_2O 0.1 to 1;

K_2O 0.1 to 1; and

Al_2O_3 1 to 5.

44. (New) The process as claimed in claim 1, wherein the glass layer has a composition, in percent by weight, comprising:

SiO_2 65 to 75;

B_2O_3 20 to 30;

Na_2O 0.1 to 1;

Li_2O 0.1 to 1;

K_2O 0.5 to 5; and

Al_2O_3 0.5 to 5.